



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of: Darrell Rinerson et al.

Attorney Docket No.: UNTYP023

Application No.: 10/605,963

Examiner: Not Yet Assigned

Filed: November 10, 2003

Group: 2818

Title: CONDUCTIVE MEMORY STACK WITH  
NON-UNIFORM WIDTH

Confirmation No.: 2962

**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on February 18, 2004 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: \_\_\_\_\_

*Laura M. Dean*  
Laura M. Dean

**INFORMATION DISCLOSURE STATEMENT  
37 CFR §§1.56 AND 1.97(b)**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

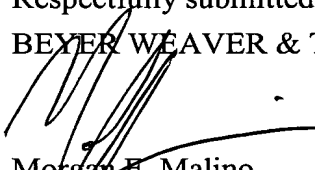
The references listed in the attached PTO Form 1449 may be material to examination of the above-identified patent application. Copies of references, except for U.S. Patents and U.S. Published Patent Applications, are enclosed. Applicants submit these references in compliance with their duty of disclosure pursuant to 37 CFR §§1.56 and 1.97. The Examiner is requested to make these references of official record in this application.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

This Information Disclosure Statement is: (i) filed within three (3) months of the filing date of the above-referenced application, (ii) believed to be filed before the mailing date of a first Office Action on the merits, or (iii) believed to be filed before the mailing of a first Office Action after the filing of a Request for Continued Examination under §1.114. Accordingly, it is believed that no fees are due in connection with the filing of this Information Disclosure

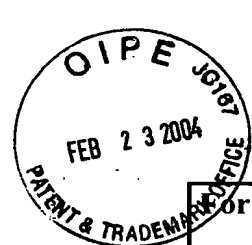
Statement. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. UNTYP023).

Respectfully submitted,  
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Form 1449 (Modified)	Atty Docket No. UNTP023	Application No.: 10/605,963
<b>Information Disclosure Statement By Applicant</b>	Applicant: Rinerson, et al.	
(Use Several Sheets if Necessary)	Filing Date November 10, 2003	Group 2818

**U.S. Patent Documents (Copies not supplied by Applicant)**

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	6,204,139	03/20/01	Liu, et al.	438	385	8/25/1998
	B	6,249,014	06/19/01	Bailey	257	295	10/1/1998
	C	6,456,525	09/24/02	Perner, et al.	365	171	9/15/2000

**Other Documents**

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	D	Beck, A. et al., " <i>Reproducible switching effect in thin oxide films for memory applications</i> ," Applied Physics Letters, Vol. 77, No. 1, 3 July 2000, 139-141.
	E	Liu, S.Q., et al., " <i>Electric-pulse-induced reversible resistance change effect in magnetoresistive films</i> ", Applied Physics Letters, Vol. 76, No. 19, 8 May 2000, 2749-2651.
	F	Liu, S.Q., et al., " <i>A New Concept For Non-Volatile Memory: Electric-Pulse Induced Reversible Resistance Change Effect In Magnetoresistive Films</i> ", Space Vacuum Epitaxy Center, University of Huston, Huston TX, 7 Pages.
	G	Park, In Seon et al., " <i>Ultra-thin EBL (encapsulated barrier layer) for Ferroelectric Capacitor</i> ," IDEM, Vol 97, 617- 620.
	H	Rossel, C. et al., " <i>Electrical current distribution across a metal-insulator-metal structure during bistable switching</i> ," Journal of Applied Physics, Vol. 90, No. 6, 15 September 2001, 2892-2898.
	I	Watanabe, Y. et al., " <i>Current-driven insulator-conductor transition and nonvolatile memory in chromium-doped SrTiO<sub>3</sub> single crystals</i> ," Applied Physics Letters, Vol. 78, No. 23, 4 June 2001, 3738-3740.
	J	Yoon, Dong-Soon et al., " <i>High Performance of Novel Oxygen Diffusion Barrier Materials for Future High-Density Dynamic Random Access Memory Devices</i> ," IEEE Transactions on Electron Devices, Vol 49, No 11, November 2002, 1917-1927.
Examiner		Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.